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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,171	02/07/2002	Masaaki Hiroki	SEL 302	1313

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COOK, ALEX, MCFARRON, MANZO,
CUMMINGS & MEHLER, LTD.
Suite 2850
200 West Adams St.
Chicago, IL 60606

EXAMINER	
NGUYEN, KEVIN M	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/072,171	HIROKI, MASAAKI	
	Examiner	Art Unit	
	Kevin M. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-11 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/2/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 2, 2007 has been entered. An action on the RCE follows:

Response to Arguments

2. This office action is made in response to applicant's amendment/argument filed on 1/2/2007. Claims 2-11 and 13-18 are amended. Applicant's argument, see pages 8-9 with respect to the amended claims 2-11 and 13-18 have been fully considered and are not persuasive. A new ground of rejection is made in view of newly found prior art references.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al (US 6,222,515) hereinafter Yamaguchi in view of Mikami et al. (US 6,825,826) hereinafter Mikami.

5. As to claim 2, Yamaguchi teaches a method of driving a liquid crystal display device (see first embodiment of Figs. 1-15F, col. 5, line 40- through col. 9, line 37), comprising:

supplying a first voltage (2V, at least one Fig. 7B) of picture signals from a source driver (8, Fig. 2) to a pixel by first scanning signals (scanning signals from a scan driver 7, Fig. 2) of a gate driver (7, Fig. 4) in a first subframe period (a first field, Fig. 7, see col. 8, lines 11-27);

supplying a second voltage (4V, Fig. 7B) of the picture signals from the source driver (8, Fig. 2) to the pixel by second scanning signals (scanning signals from a scan driver 7, Fig. 2) of the gate driver (7, Fig. 4) in a second subframe period (a second filed, Fig. 7, see col. 8, lines 11-27);

displaying one frame by displaying a first subframe and a second subframe [an average of 2V and 4V is (3V) is an image being displayed in one frame (the first and second fields), see Figs. 6 and 7B, col. 8, lines 11-15, and col. 8, lines 19-24];

wherein one frame period has the first subframe period and the second subframe period [the image of one frame (16.8ms) is divided into the first (8.4ms) and second fields (8.4ms) as shown in Fig. 6, col. 8, lines 13-15];

wherein one frame period has the first subframe period and the second subframe period are adjacent to each other [the first field and the second field are consecutive, see Fig. 7];

wherein the first voltage and the second voltage are different from each other throughout displaying the one frame [different voltage levels are applied to the first and second fields, respectively, and differences in mean effective voltage occurring in individual frames can realize more gray-scale levels that the gray-scale levels realized by applied data voltage. The image data of one display panel (the image data of one frame) can be displayed in a haft time of one frame, see col. 8, lines 28-33, and col. 7, lines 43-45].

Accordingly, Yamaguchi teaches all of the claimed limitation, except for supplying picture signals from a digital video dividing circuit to a D/A converter circuit within a source driver, and wherein the digital video data dividing circuit and the D/A converter circuit are formed on the same substrate.

However, Mikami teaches a liquid crystal display aparatus, which includes a D/A circuit 207 within a data driver circuit 307 including a high-speed data bus 203 and low-speed data bus 102 divided into block. These circuits are formed by the CMOSTET fabricating process on a glass substrate 305 of the display apparatus in figure 3, column 5 and 6 for further details of the operation.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Mikami into Yamaguchi to create the claimed invention. It would have been obvious to modify Yamaguchi to form the data driver

circuit 307 including a high-speed data bus 203 and low-speed data bus 102 divided into block, and the D/A circuit 207 on the common substrate 305 as taught by Mikami. The motivation for doing so would result in an advantage of being able not only to reduce power supply current of the D/A converting circuits but also to obtain a liquid crystal driving voltage that is stable and exhibits a less error even if the wiring resistance is high. The reason for the latter is that it is possible to reduce a voltage drop in the power supply wiring (see Mikami, col. 10, lines 26-31).

6. The limitation of claim 3 is the same as those of claim 2 and therefore the claim will be rejected using the same rationale.

7. As to claim 10, Yamaguchi teaches a liquid crystal display device comprising:

plural pixels [a plurality of pixel "P", see Fig. 2, col. 6, lines 7-11];

a gate driving circuit [a scan driver 7, Fig. 2];

a source driving circuit for supplying picture signals to the pixels by scanning signals of the gate driving circuit [a data driver (upper and lower) 8, Fig. 2, col. 6, lines 17-19];

a liquid crystal whose transmittivity is changed dependently on the voltage of the picture signals supplied to the pixels [see col. 5, lines 58-61];

means for supplying voltage of picture signals from a source driver to a pixel by scanning signals of a gate driver in each of plural subframe periods [see Figs. 7A-7D, col. 8, lines 15-27];

means for displaying one frame by displaying plural subframes [an average of 2V and 4V is (3V) is an image being displayed in one frame (the first and second fields), see Figs. 6 and 7B, col. 8, lines 11-15, and col. 8, lines 19-24];

wherein one frame period (at least one frame, Fig. 7B) has the plural subframe periods [the image of one frame (16.8ms) is divided into the first (8.4ms) and second fields (8.4ms) as shown in Fig. 6, col. 8, lines 13-15];

wherein the plural subframe periods are adjacent to each other [the first field and the second field are consecutive, see Fig. 7];

wherein the supplied voltages in adjacent subframe periods are different from each other throughout displaying the one frame [different voltage levels are applied to the first and second fields, respectively, and differences in mean effective voltage occurring in individual frames can realize more gray-scale levels that the gray-scale levels realized by applied data voltage. The image data of one display panel (=the image data of one frame) can be displayed in a haft time of one frame, see col. 8, lines 28-33, and col. 7, lines 43-45].

Accordingly, Yamaguchi teaches all of the claimed limitation, except for a digital video data driving circuit for supplying picture signals to a D/A converter circuit, and wherein the digital video data dividing circuit, the D/A converter circuit, a gate driving circuit and plural pixels are formed on the same substrate.

However, Mikami teaches a liquid crystal display apparatus, which includes a D/A circuit 207 within a data driver circuit 307 including a high-speed data bus 203 and low-speed data bus 102 divided into block, a scan driver circuit 210, and a pixel unit 209

including active matrix pixels. These circuits are formed by the CMOSTET fabricating process on a glass substrate 305 of the display apparatus in figure 3, column 5 and 6 for further details of the operation.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Mikami into Yamaguchi to create the claimed invention. It would have been obvious to modify Yamaguchi to form a data driver circuit 307 including a high-speed data bus 203 and low-speed data bus 102 divided into block, the D/A circuit 207, the scan driver circuit 210, and the pixel unit 209 on the common substrate 305 as taught by Mikami. The motivation for doing so would result in an advantage of being able not only to reduce power supply current of the D/A converting circuits but also to obtain a liquid crystal driving voltage that is stable and exhibits a less error even if the wiring resistance is high. The reason for the latter is that it is possible to reduce a voltage drop in the power supply wiring (see Mikami, col. 10, lines 26-31).

8. Claim 11 shares the same limitations as those of claim 10 and therefore the rationale for rejection will be the same.

9. Claims 4-9 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi in view of Mikami, and further in view of Katakura et al (previously cited, US 6,057,824) hereinafter Katakura.

As to claims 4-8 and 13-17, the combination of Yamaguchi and Mikami teaches all of the claimed limitations of claims 2, 3, 10 and 11, except for the frames are 1/60, 1/120, 1/24, 1/48, 1/96 second.

However, Katakura teaches a related LCD device which includes the frame frequency 20-40Hz and the frame scanning frequency 60-120 Hz (corresponding to the frames are 1/60, 1/120, 1/24, 1/48, 1/96 second, see col. 17, lines 44-47).

As to claims 9 and 18, Katakura reviews in the related art that his invention relates to a display apparatus for use in a monitor, a video camera, a projector, a television, and a car navigation system (see col. 1, lines 10-13).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Yamaguchi and Mikami to become the frame frequency 20-40Hz and the frame scanning frequency 60-120 Hz (corresponding to the frames are 1/60, 1/120, 1/24, 1/48, 1/96 second) as conventionally disclosed by Katakura in order to achieve the benefit of providing display apparatus capable of a good halftone display while suppressing the flicker (see Katakura, col. 2, lines 3-5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. NGUYEN whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, a supervisor RICHARD A. HJERPE can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see

http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Nguyen
Patent Examiner
Art Unit 2629

KMN
February 13, 2007